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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,716	10/22/2003	Nelson Gonzalez	19463-0002	3956

24633 7590 07/14/2006

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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/689,716	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,29,30,32-34,41,44-48 and 50-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,29,30,32-34,41,44-48 and 50-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's arguments with respect to claims 1-7, 29, 30, 32-34, 41, 44-48, and 50-52 have been considered but are moot in view of the new ground(s) of rejection.

2. Applicant's arguments, see pages 8-15, filed April 20, 2006, with respect to the rejection(s) of claim(s) 1-7, 29, 30, 32-34, 41, 44-48, and 50-52 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Stufflebeam (US006295566B1) and Grimaud (US005546530A).

3. With regard to Claim 1, Applicant argues that Levy (US 20040088469A1) does not teach a plurality of high speed video card slots (page 9, paragraph 2).

In reply, the Examiner disagrees. Levy discloses connecting a plurality of video cards (*comprises one or more device (DEVICES 1-5) such as video cards*, [0016]) to a plurality of ports [0020]. Since the video cards connect to these ports, these ports are considered to be high speed video card slots.

Applicant argues that Peleg (US006557065B1) does not teach that component 200 works in parallel with another video card (page 11, paragraph 1).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Stufflebeam and Grimaud.

4. With regard to Claim 2, Applicant argues that the switch 116 of Levy does not allocate bandwidth but only assists with turning the device on or off (page 13, paragraph 3).

In reply, the Examiner disagrees. Since the switch assists with turning the device on or off [0021], this means that bandwidth is either allocated or not allocated to the device, and therefore the switch allocates bandwidth.

5. With regard to Claim 41, Applicant argues that Peleg discloses two interconnects and does not disclose a single interconnect (page 15, paragraph 1).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Stufflebeam.

6. The declaration under 37 CFR 1.132 filed April 20, 2006 is insufficient to overcome the rejection of claims 1-7, 29, 30, 32-34, 41, 44-48 and 50-53 based upon Levy, Peleg, and Grimaud applied under 35 U.S.C. 103(a) as set forth in the last Office action because: The evidence supporting patentability is not sufficient to outweigh the evidence supporting prima facie case. The ultimate determination of patentability must be based on consideration of the entire record, by a preponderance of evidence, with due consideration to the persuasiveness of any arguments and any secondary evidence (*In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992)). The submission of objective evidence of patentability does not mandate a conclusion of patentability in and of itself (*In re Chupp*, 816 F.2d 643, 2 USPQ2d 1437 (Fed. Cir. 1987)). Although the record may establish evidence of secondary considerations which are

indicia of nonobviousness, the record may also establish such a strong case of obviousness that the object evidence of nonobviousness is not sufficient to outweigh the evidence of obviousness (*Newell Cos. V. Kenney Mfg. Co.*, 864 F.2d 757, 769, 9 USPQ2d 1417, 1427 (Fed. Cir. 1988), *cert. Denied*, 493 U.S. 814 (1989); *Richardson-Vicks, Inc., v. The Upjohn Co.*, 122 F.3d 1476, 1484, 44 USPQ2d 1181, 1187 (Fed. Cir. 1997)) (See MPEP 716.01(d)). The record is considered to establish a strong case of obviousness because according to Grimaud, which is one of the references relied upon, it has been known since 1994 to those of ordinary skill in the art to add video cards to card slots, wherein the video cards operate in parallel to output graphics data to a single visual display device (*a bus with card slots so that users may add processors as desired*, Col. 2, lines 40-44, *each processor is responsible only for a portion of the entire image, the buffer combines the image data from all sources into a single image frame which is then stored in a frame buffer*, Col. 2, lines 53-65; *the processors operate simultaneously on different portions of the image*, Col. 7, lines 39-40). Since this has been known since 1994 and this is similar to what Applicant is claiming, the record is considered to establish a sufficiently strong case of obviousness that the object evidence of nonobviousness is not sufficient to outweigh the evidence of obviousness.

In view of the foregoing, when all of the evidence is considered, the totality of the rebuttal evidence of nonobviousness fails to outweigh the evidence of obviousness.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-7, 29, 30, 32-34, 41, 44-48 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy (US 20040088469A1) in view of Stufflebeam (US006295566B1), further in view of Grimaud (US005546530A).

10. With regard to Claim 1, Levy describes a chipset (104, Figure 1) for managing data transfers within the computing device [0014]; a scalable interconnect (Device 0) connecting to the computing device [0021]; and a plurality of ports or high-speed video card slots [0016] connected to the interconnect [0021], the high speed video card slots including at least one first video card slot and second video card slot [0016].

However, Levy does not teach that the computing device is a motherboard and that the motherboard enables a first and a second card to attach, respectively, to the at least one first card slot and second card slot, and wherein the motherboard enables the first and the second card to operate concurrently to output data. However, Stufflebeam describes an interconnect connecting to the motherboard (*host bus 110 typically is located on a motherboard*, Col. 4, lines 48-50; *interconnection between the host bus 110, a first PCI bus 106*, Col. 4, lines 59-61); and a plurality of high-speed card slots connected to the interconnect (*PCI slots*, Col. 6, lines 23-35). Stufflebeam discloses that when the user wishes to attach an additional card, power is removed from the card slot that the card is to be attached to. After inserting the card into the slot, the software identifies and configures the additional card in the slot so that the first and second card can operate in parallel to output data (Col. 3, lines 31-33, Col. 3, line 56-Col. 4, line 17; Col. 1, lines 21-25), and the cards can include video cards (Col. 5, lines 7-19).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Levy so that the computing device is a motherboard as suggested by Stufflebeam. Motherboards are well-known in the art and widely used. Motherboards make it easy to add new features to the machine over time. Motherboards have opened the computer to creative opportunities for third-party vendors. The motherboard, by enabling pluggable components, allows users to personalize a computer system depending on their applications and needs. The advantages of using a motherboard can be found in many publications, such as the howstuffworks website. It would have been obvious to modify the device so that the motherboard enables a first and a second card to attach, respectively, to the at least one first card slot and second card slot, and wherein the motherboard enables the first and

the second card to operate concurrently to output data as suggested by Stufflebeam because Stufflebeam suggests faster processing (Col. 1, lines 21-25).

However, Levy and Stufflebeam do not specifically teach that both cards are video cards, and the video cards output graphics data to a single visual display device. However, Grimaud describes attaching a first and a second video card to at least one first video card slot and second video card slot, respectively, wherein the first and second video cards operate in parallel to output graphics data to a single visual display device (*a bus with card slots so that users may add processors as desired*, Col. 2, lines 40-44, *each processor is responsible only for a portion of the entire image, the buffer combines the image data from all sources into a single image frame which is then stored in a frame buffer*, Col. 2, lines 53-65; *the processors operate simultaneously on different portions of the image*, Col. 7, lines 39-40).

It would have been obvious to modify the devices of Levy and Stufflebeam so that a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section as suggested by Grimaud because Grimaud suggests that this ensures that a single graphics element is not overburdened with its rendering task by allowing dynamic adjustment of each graphics element so that the graphics elements take approximately the same time to render their respective images, and the video cards can operate on these divided sections in parallel, therefore allowing different graphics machines to be connected together to render complex images faster than any one of them taken separately would be able to render (Col. 5, line 55-Col. 6, line 12; Col. 7, lines 10-40).

11. With regard to Claim 2, Levy describes a switch (116, Figure 3) connected to the interconnect (Device 0), wherein the switch distributes bandwidth from the interconnect to the plurality of high-speed video card slots [0021, 0017, 0018, 0016].

12. With regard to Claim 3, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a x16 connection, and wherein the switch (116, Figure 3) distributes bandwidth from the x16 connection to two x16 video card slots [0001, 0021, 0017, 0018, 0016].

13. With regard to Claim 4, Levy describes that the interconnect comprises at least a x32 connection [0001].

14. With regard to Claim 5, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect that is divided into two or more x16 connections between the chipset (104, Figure 1) and the plurality of high-speed video card slots [0001, 0014, 0016].

15. With regard to Claim 6, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an

interconnect comprising at least a x16 connection, and wherein the interconnect is divided into a x8 connection between the chipset and each of the plurality of high-speed video card slots [0001. 0016].

16. With regard to Claim 7, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect comprising a connection having at least 24 lanes, and wherein the interconnect is divided into a x8 connection between the chipset (104, Figure 1) and one of the plurality of high-speed video card slots and a x16 connection between the chipset and another of the plurality of high-speed video card slots [0001, 0016].

17. With regard to Claim 29, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses that the interconnect comprises a first x16 connection to the first video card slot and a second smaller-scaled connection to the second video card slot [0001, 0016].

18. With regard to Claim 30, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Levy gives an example

wherein the second connection is a x4 connection. Therefore, Levy discloses a second connection that is at least one of a x1, x2, x4, and x8 connection [0001].

19. With regard to Claim 32, Levy describes ports or a peripheral slot connected to the interconnect (Device 0, Figure 2). In Figure 2, the peripheral slot is shown to have the prespecified dimensions a x8 link, and the first dimensions are for a x4 link and a x8 link [0020]. Therefore, Levy discloses a peripheral slot having second prespecified dimensions, wherein the second dimensions differs from the first dimensions.

20. With regard to Claim 33, Levy describes that a graphics card can be coupled to any of the video card slots [0016, 0020]. Therefore, Levy discloses first dimensions of the video card slots that are selected to allow a graphics card to be coupled to any of the video card slots.

21. With regard to Claim 34, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses a graphics card that is designed to be used with a x16 connection [0001, 0016].

22. With regard to Claim 41, Levy describes a computing device for supporting multiple video cards, the computing device comprising a processor socket (104, Figure 1) adapted to receive a processor (102) [0014]; a single scalable interconnect (Device 0) that provides data paths to the processor socket (Figure 1), wherein the scalable interconnect is selectively divided

as needed to allocate the data paths [0016-0017]; and a plurality of high-speed video card slots connected to the interconnect, wherein each of the video card slots has first prespecified dimensions and is specifically adapted for coupling to a video card [0001, 0021, 0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data. However, Stufflebeam describes that the computing device is a motherboard (Col. 4, lines 48-50), the processor is a central processing unit (CPU) (100, Figure 1; Col. 4, lines 40-46), and the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data (Col. 3, lines 31-33, Col. 3, line 56-Col. 4, line 17; Col. 1, lines 21-25), wherein the cards can include video cards (Col. 5, lines 7-19).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Levy so that the processor is a CPU as suggested by Stufflebeam. CPUs are well-known in the art and are widely used. The CPU is the brains of the computer. The CPU is needed to perform most of the calculations. In terms of computing power, the CPU is the most important element of a computer system. This can be found in many publications, such as the Webopedia Online Encyclopedia. It would have been obvious to modify the device so that the motherboard is capable of receiving and facilitating concurrent operation of a first and a second card to output data for the same reasons given in the rejection for Claim 1.

However, Levy and Stufflebeam do not teach that the cards are substantially similar video cards and operate to output graphics data to a single visual display device. However,

Grimaud discloses the cards are substantially similar video cards and operate to output graphics data to a single visual display device (Col. 2, lines 40-44; Col. 2, lines 53-65; Col. 7, lines 39-40). This would be obvious for the same reasons given in the rejection for Claim 1.

23. With regard to Claim 44, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses that each of the video card slots is configured to couple with a graphics card designed to be used with a x16 connection [0001, 0016].

24. With regard to Claim 45, Levy describes that the interconnect supports links between chips that may comprise x1, x2, x4, x8, x12, x16, or x32 lanes, and requires chips to support at least x1 links, leaving chips to optionally support the other link widths. Therefore, Levy discloses an interconnect (Device 0, Figure 1) comprising a first data path (Link 1) and a second data path (Link 2), each of the first and second data paths connecting the processor socket (104) to different video card slots, the first data path being equal to or larger in scale than the second path [0001, 0016].

25. With regard to Claim 46, Claim 46 is similar in scope to Claim 30, and therefore is rejected under the same rationale.

26. With regard to Claim 47, Claim 47 is similar in scope to Claim 32, and therefore is rejected under the same rationale.

27. With regard to Claim 48, Levy describes a high performance computer including a scalable interconnect (Device 0) including a first and a second provides data paths, wherein the scalable interconnect is selectively divided as needed to allocate the data paths [0016-0017], and a first and a second video slots, wherein the first and the second video slots connect, respectively, to the first and second data paths [0020], the first data path being equal to or larger in scale than the second data path, wherein the first and the second video slots have a substantially similar physical configuration [0001], as discussed in the rejection for Claim 42, and wherein the video slot physical configuration is selected to allow the first and the second video slots to accept a graphics card; and a first graphics card coupled to the first video slot [0016].

However, Levy does not teach that the computing device is a motherboard, the processor is a central processing unit (CPU), and a second graphics card coupled to the second video slot, wherein first and second video cards operate concurrently to output graphics data to a display device. However, Stufflebeam describes that the computing device is a motherboard (Col. 4, lines 48-50), the processor is a central processing unit (CPU) (100, Figure 1; Col. 4, lines 40-46), and a second card coupled to the second slot, wherein first and second cards operate concurrently to output data (Col. 3, lines 31-33, Col. 3, line 56-Col. 4, line 17; Col. 1, lines 21-25), wherein the cards can include video cards (Col. 5, lines 7-19). This would be obvious for the same reasons given in the rejection for Claim 41.

28. With regard to Claim 50, Levy does not teach that a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section. However, Grimaud describes a display area of the display device is divided into first and second sections, the first video card performing graphics processing related to the first section; and the second video card performing graphics processing related to the second section (Col. 2, lines 40-44, 53-65). This would be obvious for the same reasons given in the rejection for Claim 1.

29. With regard to Claim 51, Claim 51 is similar in scope to Claim 50, and therefore is rejected under the same rationale.

30. With regard to Claim 52, Claim 52 is similar in scope to Claim 50, and therefore is rejected under the same rationale.

Prior Art of Record

Gary Brown, "How Motherboards Work",
http://electronics.howstuffworks.com/motherboard.htm/printable.

"CPU", http://www.webopedia.com/TERM/C/CPU.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH

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